PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Peter Warnes, et al.	)
			)
Appl. No.	:	09/523,877	)
			)
Filed	:	March 13, 2000	)
			)
For	:	**METHOD AND APPARATUS FOR MULTI-MODE JUMP DELAY SLOT CONTROL IN A PIPELINED PROCESSOR**	))))
			)
Examiner	:	Huisman, David	)
			)
Group Art Unit:		2183	))

AMENDMENT AND RESPONSE TO OFFICE ACTION

RECEIVED

MAR 2 8 2003

Technology Center 2100

10   Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

15   In response to the Office Action dated December 16, 2002 for the above-identified application ("Office Action"), Applicant provides the following:

RESTRICTION ELECTION

20   Applicant herein elects without traverse the invention of Group I, drawn to a processor and method for executing branch/jump instructions, per page 2, Par. 1 of the Office Action. Applicant herein cancels Claims 6-11, 22 and 24 without prejudice.

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METHOD AND APPARATUS FOR MULTI-MODE JUMP DELAY SLOT
CONTROL IN A PIPELINED PROCESSOR

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This application claims priority to U.S. Provisional Patent Application Serial No. 60/134,253 filed May 13, 1999, entitled "Method And Apparatus For Synthesizing And Implementing Integrated Circuit Designs".

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Related Applications

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This application is related to co-pending U.S. Patent Application Serial No. 09/523,871 filed March 13, 2000 and entitled "Method and Apparatus for Jump Control in a Pipelined Processor", U.S. Patent Application Serial No. 09/524,179 filed March 13, 2000 and entitled "Method and Apparatus for Processor Pipeline Segmentation and Re-Assembly", U.S. Patent Application Serial No. 09/524,178 filed March 13, 2000 and entitled "Method and Apparatus for Loose Register Encoding Within a Pipelined Processor", and U.S. Patent Application No. 09/418,663 filed October 14, 1999, entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design".